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Low-Power Dynamic Logic Multiband Flexible Integer-N Divider for WLAN Frequency Synthesizers Using a 32/33/47/48 Multimodulus Prescaler

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Abstract: *Multiband wireless transceivers require frequency synthesizers capable of supporting more than one operating band without a proportional increase in power, area, and clock-distribution complexity. This paper presents a low-power single-phase-clock flexible integer-N divider based on pulse-swallow architecture. The design integrates a wideband 2/3 prescaler, a 32/33/47/48 multimodulus prescaler, a 7-bit programmable P-counter, and a 6-bit swallow S-counter. The central low-power mechanism suppresses unnecessary switching and short-circuit current in the first flip-flop path during divide-by-2 operation, while the multimodulus stage extends the divider to both the 2.4-GHz and 5–5.825-GHz bands without adding another prescaler flip-flop. The source design reports more than 50% prescaler power saving in divide-by-2 mode and a 6.5-GHz maximum operating frequency for the wideband prescaler. The architecture was modeled in Verilog HDL, functionally evaluated in ModelSim, and synthesized using Xilinx ISE. The supplied FPGA synthesis report indicates a 4.187-ns minimum clock period (238.829 MHz), 1026 slice registers (5%), and 3562 slice LUTs (18%) on an XC5VLX30-3-FF324 target. The results demonstrate the structural feasibility of a programmable single-clock multiband divider, while also revealing that the current top-level FPGA test configuration must be reduced or serialized to satisfy physical I/O limits.*

Keywords: Frequency Synthesizer, PLL, WLAN, TSPC, E-TSPC, Prescaler, Pulse-Swallow Divider, Multimodulus Divider, Low-Power VLSI, Verilog, FPGA.

I. Introduction

Wireless local-area networks and short-range wireless systems require frequency synthesizers that can generate stable channel frequencies while meeting strict power and integration constraints. The underlying project targets multiband operation associated with IEEE 802.11a/b/g-class WLAN systems and IEEE 802.15.4-class low-rate systems. In a conventional RF phase-locked loop (PLL), the feedback divider is among the most active digital blocks because it operates at or near the voltage-controlled oscillator frequency. Consequently, the first-stage frequency divider can dominate the digital power budget of the synthesizer [1]– [3].

High-speed source-coupled-logic dividers achieve multi-gigahertz operation but consume relatively high static power. Dynamic single-phase clocked logic, particularly true single-phase clock (TSPC) and extended-TSPC (E-TSPC), offers an attractive alternative because only one clock phase is required and

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clock-skew management is simplified [5], [6]. However, the source report identifies a key trade-off: E-TSPC can provide higher operating frequency through reduced load capacitance, but short-circuit power becomes significant; TSPC can reduce short-circuit power but may incur higher switching power because of larger capacitive loading. The objective of this work is therefore to construct a fully programmable multiband integer-N divider that retains the speed advantages of dynamic logic while suppressing unnecessary switching activity [7]. The architecture combines a wideband 2/3 prescaler with a 32/33/47/48 multimodulus stage, followed by programmable P and S counters. A band-selection signal reconfigures the divider between the 2.4-GHz region and the 5–5.825-GHz region, enabling one divider structure to serve multiple communication bands.

II. Background and Design Motivation

2.1 Power in High-Speed CMOS Dividers: For high-speed CMOS digital circuits, propagation delay and power dissipation are tightly coupled design constraints. The source design characterizes the maximum operating frequency from the low-to-high and high-to-low propagation delays:

$$Fmax = \frac{1}{(tpLH + tpHL)} \quad (1)$$

The dynamic switching component increases with clock frequency, effective load capacitance, and the square of the supply voltage. For the set of switching nodes in the divider, the source formulation can be written as:

$$Psw = fclk \cdot \Sigma\, CL,i \cdot VDD^2 \quad (2)$$

A second contribution is short-circuit power, produced when a direct current path temporarily exists between the supply rails during a logic transition:

$$PSC = ISC \cdot VDD \quad (3)$$

The proposed low-power strategy is based on eliminating or freezing internal transitions whenever a logic block is not required for the current division mode. This is particularly effective in the 2/3 prescaler because divide-by-2 operation can be achieved with only the second dynamic flip-flop actively switching.

2.2 TSPC and E-TSPC Considerations: TSPC registers use a single clock phase and can embed Boolean logic into the latch structure, thereby reducing the delay overhead of separate combinational gates. The source report notes that E-TSPC reduces capacitive loading and can operate faster but also experiences larger short-circuit power. This motivates the use of a modified wideband single-phase prescaler that selectively disables the unnecessary current paths instead of relying on a conventional E-TSPC 2/3 cell.

III. Proposed Multiband Flexible Divider

Figure 1 shows the complete pulse-swallow architecture. The input is first processed by a multimodulus 32/33/47/48 prescaler. Its output clocks a 7-bit programmable P-counter and a 6-bit

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swallow S-counter. The MOD feedback signal controls whether the prescaler remains in the N or N+1 division state, while the Sel signal determines the low-band or high-band multimodulus configuration.

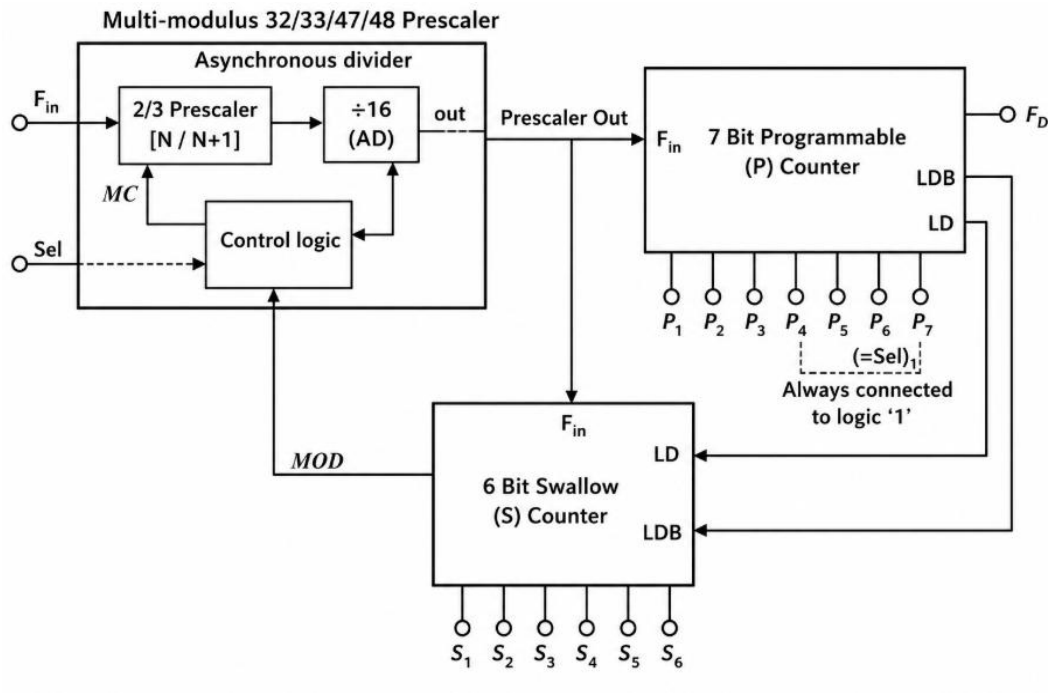

Figure 1: Proposed dynamic-logic multiband flexible divider architecture

Table 1: Functional role and programming ranges of the proposed divider blocks

Block	Function	Low-band Setting	High-band Setting
2/3 Prescaler	First high-speed divide stage	÷2/÷3	÷2/÷3
Multimodulus Prescaler	Extends first stage to pulse-swallow ratios	32/33	47/48
P-counter	Programs coarse division count	75–78	105–122
S-counter	Programs swallow count	0–31	0–47
Sel	Band-selection control	2.4-GHz band	5–5.825-GHz band

3.1 Wideband 2/3 Prescaler: The wideband 2/3 prescaler uses two D flip-flops with NOR functions embedded in the dynamic stages. The control signal MC selects the required division ratio. During divide-by-2 operation, internal nodes of the first flip-flop are forced to logic zero and remain inactive; as a result, switching in that path is removed and one transistor in each affected stage remains off, making the short-circuit component negligible in those stages.

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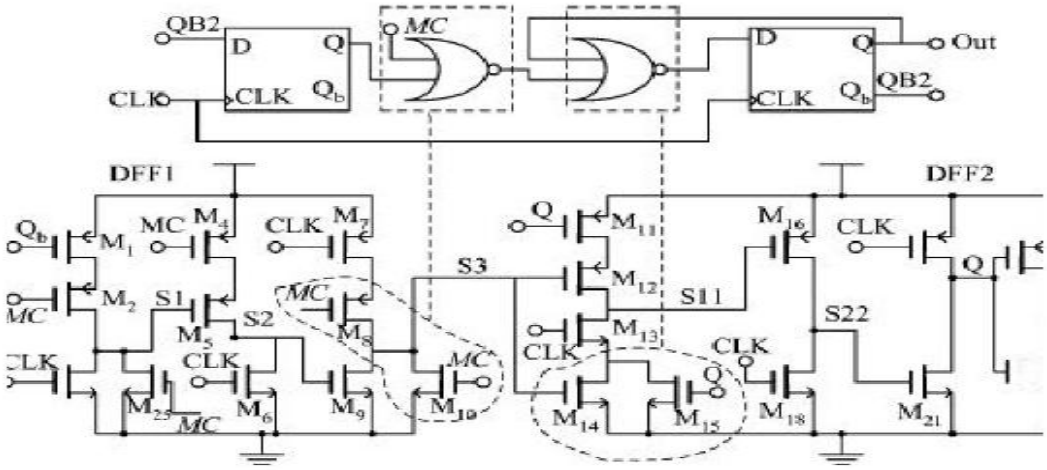

Figure 2: Wideband single-phase-clock 2/3 prescaler used by the proposed divider

Only the second flip-flop actively contributes to switching activity during the divide-by-2 state. The supplied report therefore attributes more than 50% power saving to this operating mode and states that the wideband prescaler can reach a maximum operating frequency of 6.5 GHz. When MC changes to the complementary state, the logic value from the first flip-flop is transferred forward and the prescaler operates in divide-by-3 mode.

3.2 Multimodulus 32/33/47/48 Prescaler: The multimodulus stage reuses the 2/3 prescaler together with four asynchronous divide-by-2 TSPC stages and a compact set of combinational gates. An additional inverter and 2:1 multiplexer allow the same chain to produce 32/33 or 47/48 division without introducing another flip-flop.

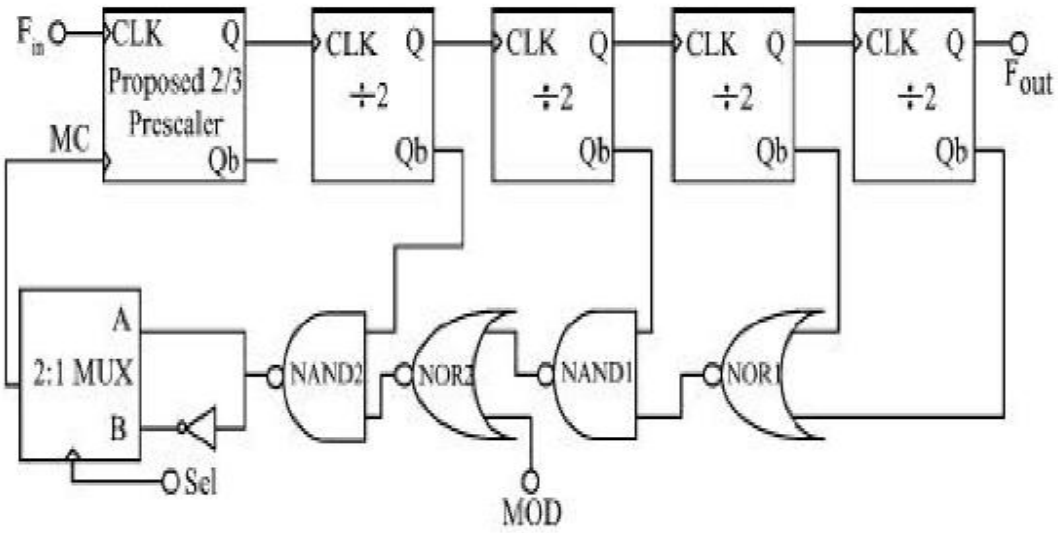

Figure 3: Wideband multimodulus 32/33/47/48 prescaler

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For Sel = 0, the logic behaves as a conventional 32/33 prescaler. With AD = 16 and the basic prescaler division N1 = 2, the divide-by-32 condition follows:

$$N = AD \cdot N1 = 16 \cdot 2 = 32 \qquad (4)$$

Activating the swallow condition inserts one divide-by-3 event and produces the adjacent ratio of 33. For Sel = 1, the control path is inverted so that the first-stage prescaler is biased toward divide-by-3. The corresponding high-band ratios are:

$$N + 1 = AD \cdot (N1 + 1) = 16 \cdot 3 = 48 \qquad (5)$$

$$N = (AD - 1)(N1 + 1) + N1 = 15 \cdot 3 + 2 = 47 \qquad (6)$$

Thus, the same divider backbone supports four adjacent division ratios. This arrangement reduces counter complexity in the high-frequency band because a fixed 32/33 prescaler would otherwise require a larger programmable counter range.

3.3 Pulse-swallow P- and S-counter Operation: The 6-bit S-counter is constructed from asynchronous loadable bit cells, a NOR-embedded flip-flop, and supporting logic. The counter determines how long the prescaler operates in its N+1 mode. After the S-count is exhausted, MOD changes state and the prescaler returns to N mode for the remaining P–S count. During this interval the S-counter is intentionally held inactive, suppressing switching power for N(P–S) prescaler clock cycles.

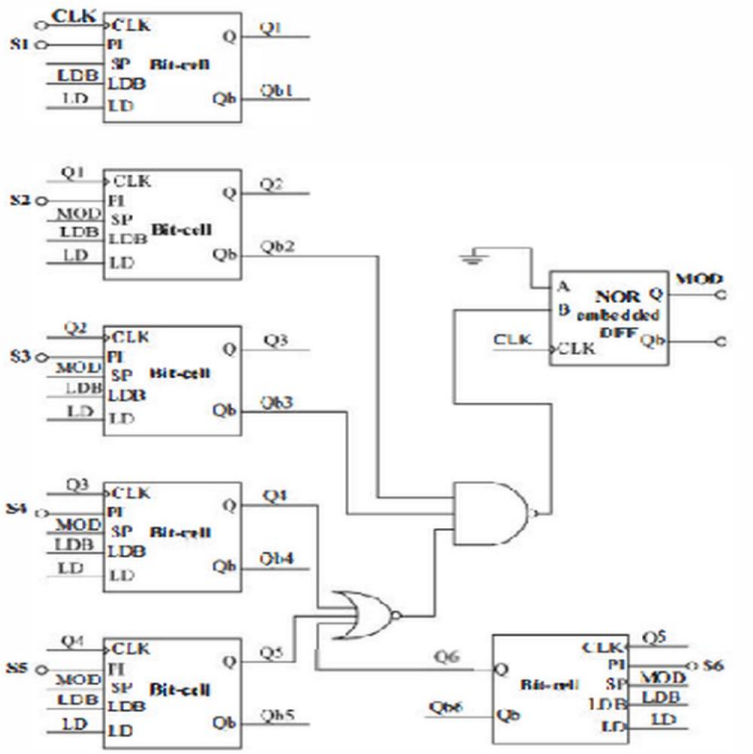

Figure 4: Asynchronous 6-bit swallow S-counter with MOD-controlled low-power bit cells

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The 7-bit P-counter is an asynchronous down counter implemented with loadable bit cells. It is programmed from 75 to 78 in the lower band and from 105 to 122 in the upper band. At the end of the P-count, the load signal reloads both counters and restores the initial MOD state. From the pulse-swallow sequence, the effective divider ratio can be expressed as:

$$D = S(N + 1) + (P - S)N = NP + S \qquad (7)$$

Equation (7) clarifies why the programmable S-count provides fine frequency steps while P provides the coarse division range. Replacing N with either 32/47 and selecting the associated N+1 value gives a unified mechanism for multiband channel programming.

IV. RTL Implementation and Verification Methodology

The divider was described at register-transfer level in Verilog HDL. The supplied project uses ModelSim 6.4c for functional verification and Xilinx ISE 13.2/XST for synthesis. A typical verification sequence consists of library creation, HDL compilation, top-level loading, stimulus application, waveform inspection, and debugging. The synthesis stage maps the RTL to the selected FPGA primitives and performs timing analysis.

4.1 Verification Sequence: Model each divider block in Verilog HDL and verify local divide/control behavior.

1. Integrate the 2/3 prescaler, multimodulus logic, P-counter, S-counter, and control feedback.
2. Apply clock, reset, band-select, and programming stimuli in the testbench.
3. Inspect counter reload, MOD transition, and output division behavior in ModelSim.
4. Synthesize the integrated RTL with Xilinx XST for an XC5VLX30-3-FF324 target.
5. Review utilization, timing, warnings, and implementation feasibility.

The design flow separates two different performance domains. The source's 6.5-GHz value refers to the wideband prescaler behavior discussed at the transistor/dynamic-logic level, whereas the Xilinx synthesis timing reflects an FPGA-mapped RTL implementation. These values should not be interpreted as contradictory because FPGA LUT/routing delays and I/O structures are fundamentally different from a custom CMOS prescaler.

V. Results and Discussion

5.1 Functional and Architectural Observations: The architecture provides four prescaler ratios using one first-stage wideband prescaler and one asynchronous divide chain. In low-band operation, Sel selects the 32/33 path; in high-band operation, Sel selects 47/48. The S-counter generates the MOD transition that changes from N+1 operation to N operation, and the P-counter generates the reload event. This organization eliminates the need for separate dedicated divider chains for each band.

The source simulation section contains RTL schematic and waveform screenshots produced in the Xilinx/ModelSim environment. Figure 5 reproduces the synthesis summary from the project, while Fig. 6 shows the simulation environment and representative clock/control activity used during verification.

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Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1026	19200	5%
Number of Slice LUTs	3562	19200	18%
Number of fully used LUT-FF pairs	1023	3565	28%
Number of bonded IOBs	2085	220	947%
Number of BUFG/BUFGCTRLs	1	32	3%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Aug 8 11:33:15 2014	0	2 Warnings	0
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

Figure 5: Xilinx synthesis/device-utilization summary from the supplied implementation

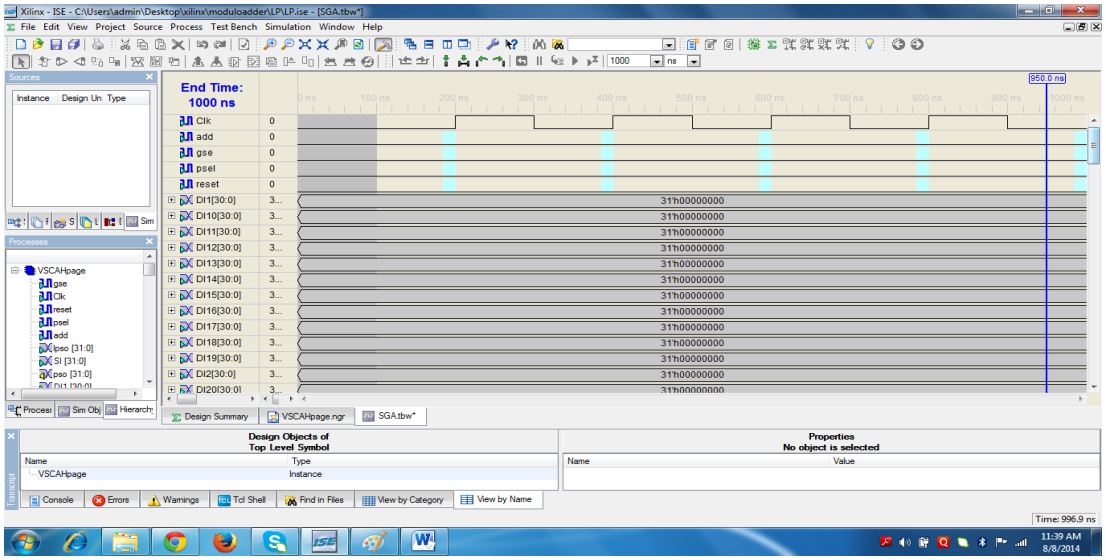

Figure 6: Representative RTL simulation waveform and test activity from the supplied implementation

5.2 FPGA Synthesis Results:

Table 2: Key FPGA synthesis and timing results reported in the supplied project

Metric	Reported Value	Interpretation
Target FPGA	XC5VLX30-3-FF324	Virtex-5 target used by XST
Slice registers	1026 / 19200 (5%)	Low sequential resource occupancy
Slice LUTs	3562 / 19200 (18%)	Moderate combinational occupancy
Fully used LUT–FF pairs	1023 / 3565 (28%)	Partial packing opportunity remains

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BUFG/BUFGCTRL	1 / 32 (3%)	Single global clock resource
Minimum clock period	4.187 ns	Post-synthesis timing estimate
Maximum clock frequency	238.829 MHz	FPGA-mapped RTL timing
Maximum combinational path delay	6.770 ns	Longest reported combinational path
Synthesis status	0 errors, 2 warnings	Compilation successful with warnings

The XST timing report gives a minimum period of 4.187 ns, equivalent to 238.829 MHz for the synthesized top-level clock. The maximum combinational path delay is 6.770 ns. Resource utilization is modest for registers and LUTs, which indicates that the core logic does not exhaust the selected Virtex-5 fabric.

5.3 Important Implementation Limitation: I/O Over-utilization: The supplied synthesis report also shows 2085 bonded I/Os requested for a device with 220 bonded IOBs, i.e., 947% of the available package I/O capacity. XST explicitly issues a resource-overutilization warning. This does not invalidate the divider logic itself, but it means the current top-level verification wrapper is not directly place-and-routable on the selected package. For a physical FPGA prototype, wide internal test vectors should be kept inside the device, observed through an embedded logic analyzer, multiplexed across a smaller debug bus, or serialized.

5.4 Power and Scalability Discussion: The primary low-power gain is architectural rather than tool-specific. In divide-by-2 mode, the first dynamic flip-flop path is prevented from switching; when the S-counter is inactive after the swallow interval, its internal nodes are similarly clamped. Because switching power grows linearly with activity and clock frequency, disabling high-rate internal transitions is especially valuable in a PLL feedback divider.

The multimodulus 32/33/47/48 stage further reduces system-level complexity by sharing one divider chain between low and high bands. The design therefore targets the same objective as multiband frequency synthesizers reported in [1]–[3], while using dynamic single-phase logic to reduce divider power and clocking overhead.

VI. Design Advantages and Engineering Trade-offs

Table 3: Architectural Advantages and Practical Trade-offs

Design Aspect	Proposed Approach	Engineering Implication
Clocking	Single-phase dynamic logic	Avoids complementary-clock skew management
First-stage division	2/3 prescaler with switching suppression	Reduces active dynamic nodes in divide-by-2 mode

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Multiband support	32/33/47/48 multimodulus ratios	One divider architecture supports two band groups
Programming	7-bit P + 6-bit S counters	Fine integer-N channel programmability
Counter power	MOD-controlled inactive nodes	Reduces switching after S-counter reaches zero
Hardware complexity	No extra FF for 47/48 extension	Lower multimodulus structural overhead
FPGA prototype	RTL synthesis successful	Requires I/O-wrapper redesign before physical implementation

A notable trade-off is that the original low-power claims are fundamentally associated with transistor-level dynamic logic, whereas a generic FPGA implementation maps the design into LUTs and flip-flops. The FPGA results are therefore best used for RTL functional validation and digital timing feasibility; silicon power and multi-gigahertz operation require transistor-level SPICE simulation and custom-layout verification.

VII. Limitations and Future Work

The present evidence set combines dynamic-CMOS architectural analysis with RTL/FPGA synthesis. A publication-grade silicon claim would require a unified evaluation flow that includes transistor-level post-layout simulation or fabricated measurements of prescaler power, phase noise/jitter contribution, duty-cycle behavior, and operating range across process, voltage, and temperature corners. The current report does not provide these measurements.

Future work should therefore (i) implement the 2/3 and 32/33/47/48 stages in a modern CMOS PDK; (ii) perform extracted post-layout simulations; (iii) quantify power separately for divide-by-2, divide-by-3, low-band, and high-band operation; (iv) measure divider-induced jitter and input sensitivity; (v) reduce the FPGA top-level I/O count for a real hardware prototype; and (vi) compare power-delay product against conventional SCL, TSPC, and E-TSPC divider baselines under identical conditions.

VIII. Conclusion

A low-power multiband flexible integer-N divider for WLAN-oriented frequency synthesis has been presented. The architecture combines a wideband single-phase 2/3 prescaler, a 32/33/47/48 multimodulus stage, a programmable 7-bit P-counter, and a 6-bit swallow S-counter. Power reduction is obtained by suppressing switching and short-circuit paths in inactive dynamic stages, while the multimodulus extension provides low- and high-band operation without an additional divider flip-flop. The source design reports more than 50% power saving during divide-by-2 operation and a 6.5-GHz wideband-prescaler operating limit. The Verilog implementation was simulated and synthesized with Xilinx tools; the supplied report shows 238.829-MHz FPGA timing with 5% slice-register and 18% LUT usage, but also exposes an oversized top-level I/O wrapper that must be redesigned before place-and-route. Overall, the work provides a compact and technically meaningful basis for a low-power multiband PLL feedback divider and a clear path toward a stronger ASIC-oriented implementation.

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